



03
03.2002

PATENT APPLICATION
2207/11273

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: FLETCHER et al

Application No.: 09/893,871

Group Art Unit: 2182

Examiner: Not assigned

Filed: June 29, 2001

For: MULTISTAGE CLOCK DELAY CIRCUIT AND METHOD

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Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The paragraphs marked below are applicable.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☐ 2. This Information Disclosure Statement is being filed with a Request for Continued Examination (RCE). No certification or fee is required.

☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☐ c. Please debit Deposit Account No. 11-0600 in the amount of \$240.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

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Respectfully submitted,

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Date: Feb. 28, 2002



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 1

Complete if Known

Application Number	09/893,871
Filing Date	June 29, 2001
First Named Inventor	FLETCHER et al
Group Art Unit	2182
Examiner Name	Not assigned
Attorney Docket Number	2207/11273

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,208,907 B1	03/27/2002	DURHAM et al	

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FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430	
		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996	
		Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000	
		Presentation by Carl Sechen dated March 17, 2000.	
		Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, McGraw-Hill, 1982	

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